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1. Your reference

TMG/P70528

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2. Patent application number
   (The Patent Office will fill in this part)

   9914380.2

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3. Full name, address and postcode of the or of each applicant *(underline all surnames)*

   TIMOTHY JAMES REGAN
   27 MARKET PLACE
   OLNEY
   BUCKINGHAMSHIRE MK46 4AJ

   Patents ADP number *(if you know it)*

   If the applicant is a corporate body, give the country/state of its incorporation

   767362 0001

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4. Title of the invention

   METHOD OF SCALING AN INTEGRATED CIRCUIT

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5. Name of your agent *(if you have one)*

   "Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*

   T M GREGORY & CO.
   26 CYRIL STREET
   NORTHAMPTON NN1 5EL

   4323 0001

   Patents ADP number *(if you know it)*

   692748001

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6. If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and *(if you know it)* the or each application number

Country	Priority application number *(if you know it)*	Date of filing *(day / month / year)*

---

7. If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application

Number of earlier application	Date of filing *(day / month / year)*

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   a) *any applicant named in part 3 is not an inventor, or*
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Statement of inventorship and right to grant of a patent (Patents Form 7/77)	–
Request for preliminary examination and search (Patents Form 9/77)	–
Request for substantive examination (Patents Form 10/77)	–
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11.

I/We request the grant of a patent on the basis of this application.

Signature

T M GREGORY & CO

Date 21.06.99

12. Name and daytime telephone number of person to contact in the United Kingdom

T M Gregory (01604 632436)

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METHOD OF SCALING AN INTEGRATED CIRCUIT

The present invention relates to a process by which the physical design or layout of an integrated circuit can be modified to meet a different set of design and manufacturing rules. This method involves analysing data of the existing integrated circuit to determine the scaling factor then altering the shapes in the original by scaling the data, scaling individual layers, adjusting the edges of shapes and swapping geometries and cells through a defined sequence, according to a process migration technique.

It is known from, for example, US 5640497 to provide a method of redesigning layouts. However, such methods are not always effective. Hence it is an object of the present invention to provide a different process migration technique which may be described as "complex scaling" and which is applicable to the computer model of the layout of any existing integrated circuit. By using this technique, the layout of a chip may be modified to be manufactured in any new process and at any scale that meets the new design rules.

The method is applicable to flat chip layouts and those containing design hierarchy, which may be defined as the placing of sub-cells into higher level circuits and these, in turn, being placed again. The hierarchy of the migrated chip matches the hierarchy of the original.

According to the present invention, there is provided a method of scaling an integrated circuit comprising the steps of examining the existing layout to determine the amount by which the layout must be scaled, including determining variable geometry values; absolute geometry values; and a design grid, and carrying out one or more of gate width and length adjustment;

layer scaling; polygon edge adjustment; contact replacement; adjust overlaps; addition or removal of layers; cell swapping; and verification.

An embodiment of the invention will now be more particularly described by way of example and with reference to the accompanying drawings, in which:

Figure 1 shows circuit hierarchy where building blocks of circuitry are placed into larger blocks which can be placed again into yet larger blocks;

Figure 2 shows variable rule examples, where geometry must be equal to or greater than a set distance and width;

Figure 3 shows fixed geometry value examples, where geometry dimensions must equal a defined value;

Figure 4 shows interconnect spacing;

Figure 5 shows via geometries and arrays;

Figures 6A and 6B show CMOS transistor geometry;

Figures 7A and 7B show general scaling;

Figure 8 shows CMOS transistor definition and value definition;

Figure 9 shows CMOS transistor edge adjustment;

Figure 10 is illustrative of layer shrinking breaking connectivity;

Figure 11 illustrates hierarchical layer shrink with connectivity;

Figure 12 shows layer sizing by geometry width;

Figure 13 shows edge adjustment for transistors;

Figure 14a shows contact shapes in a layout;

Figure 14b shows removing and replacing contact shapes;

Figure 14c shows identifying areas requiring contacts with Boolean functions;

Figure 15 shows layer overlap;

Figure 16 shows new well defined around existing diffusion;

Figure 17 shows routing information from metal 1 promoted to metal 3;

Figure 18a shows cell swapping in a standard cell layout;

Figure 18b shows cell swapping in a block based layout; and

Figure 19 shows standard cells containing feedthrough ports.

The technique for modifying the circuit involves a series of steps that scale the data and modify the shapes contained within it to comply with a set of design rules that govern the manufacturing process for production of the finished chip.

The techniques contained in this process will work for all components and connection geometries on a chip including, but not restricted to, MOSFET and bipolar transistors, resistors, capacitors and diodes.

The input data for the process migration can be any existing chip or IC layout or the intellectual property contained therein, in an industry standard format such as GDSII or CIF. These files will contain the data that makes up the chip and may include rectangles, polygons, paths, instances, arrays and labels.

A modification sequence will include some or all of the following:-
Design analysis and scaling calculations;
General scaling;
Gate width and length adjustment;
Layer scaling;
Polygon edge adjustment;
Contact replacement;
Adjust overlaps;
Addition or removal of layers;
Cell swapping;
Verification.

In order to apply a factor to the general scaling calculations it is necessary to examine the existing layout to determine the amount by which the layout must be scaled. There are three factors that must be taken into account in this process:-

1. Variable geometry values;
2. Absolute geometry values;
3. The design grid.

Taking the first of these, namely variable geometry values, many of the design rules in an integrated circuit manufacturing process are given as a minimum value and may be exceeded when designing the circuit. An example of this would be a rule that determines the spacing between two geometries on the same layer that is enforced to ensure that the two geometries do not merge together during manufacture. The spacing rule may be exceeded as long as the minimum value given is not violated.

Examples of variable geometry values include widths, spacings and enclosures of layers.

Figure 2 shows variable rule examples, where geometry must be equal to or greater than a set distance and width.

The second factor relates to absolute geometry values. Integrated circuit design rules usually have fixed values for certain geometries that must be met and cannot be exceeded. These are usually applied to contact and via holes that connect routing circuitry and this value must be met for each occurrence of these shapes. In addition, transistor sizes are defined in the circuit net list and this must be matched in the layout. Failure to meet these values will result in errors when checking the layout against the schematic.

Examples of fixed values include contact and via sizes, transistor sizes, resistor sizes and capacitor sizes, and in Figure 3, fixed geometry value examples are shown, where geometry dimensions must equal a defined value.

Finally, all integrated circuits are designed to have the coordinates of each shape as a multiple of a pre-defined grid. The scaling factor must take the new design grid into account. This can be accomplished in two ways, by calculating the scaling factor to ensure that the coordinates of all shapes in the scaled layout fall on grid, or snapping coordinates to grid as they are scaled. All coordinates in the final chip must be placed on the defined design grid.

The scale factor for any process migration will be calculated from the ratio between the rules in the new manufacturing process specification and the rules used in the original device. There are three distinct parts of a chip that can be the limiting factor in scaling the design and

the ratio of each must be calculated.. The largest of the three ratios will be defined as the limiting factor in scaling the chip.

1. Interconnect scaling.

The width and spacing for each routing layer must be calculated as a ratio defined by:-

(new width + new spacing) / (old width + old spacing)

Figure 4 shows interconnect spacing.

2. Via size.

The size of the fixed rectangles that make up the via holes between routing layers:-

Max ((new via 1 / old via 1)

(new via 2 / old via 2) .....)

Figure 5 shows via geometries and arrays.

3. Transistor geometry.

The relative shrink of the shapes that make up the distance between two transistors in separate pieces of diffusion:-

New (2a + 2b + 2c + 2d + e)/Old (2a + 2b + 2c + 2d +e)

Figures 6A and 6B show CMOS transistor geometry.

The maximum value derived from these calculations will determine the scaling factor. This scaling factor must be rounded up to the next whole grid point, i.e. mod(scale grid)= 0.

A fourth factor that may need consideration concerns circuits that contain resistors and capacitors. These need to be scaled depending on the values of the materials used to construct them in the two manufacturing processes. Resistors and capacitors are defined by the value per square unit of the materials used in their construction. The ratio of these values in the old and new manufacturing process is used to calculate the scaling factor for these circuit components.

Once the scaling factor has been determined, it is applied to each cell and geometry in the whole chip. Each coordinate is multiplied by the scaling factor to reduce the chip in size while keeping the geometries and hierarchy of the chip intact. At this stage, the new chip will be identical to the old in everything but scale.

The scaling of geometries and cells may be defined as coordinate scaling.

In the general scaling process each shape within the layout will be adjusted relative to the origin of the chip's axis, i.e. $x = 0$, $y = 0$.

Figure 7 shows general scaling.

The SEMOS transistors in a circuit are determined by the overlap of two materials, doped silicon, known as diffusion, and polysilicon or occasionally metal. When scaling the width and length of a transistor, it is not possible to apply an absolute value to every diffusion and polysilicon polygon through the layout. Instead, the diffusion and polysilicon that make up the width and length of the transistor must change by a percentage of the transistor size and so each one must be scaled in turn and adjusted as a multiple of its current size. This involves the use of an edge scaling method that identifies the edges of diffusion that make up each transistor's width and length and moving them to meet the new value. Edge adjustment can be considered as being distinct from scaling.

The individual transistors are identified with a Boolean operation that places shapes over any area where polysilicon crosses diffusion. These shapes will form the basis for the rest of the transistor sizing operations in a circuit containing CMOS transistors.

Figure 8 shows CMOS transistor definition and value definition.

The diffusion and polysilicon edges that make up the transistor are selected and moved by a percentage of the gate width or length to adjust the value of the transistor. One piece of diffusion may make up several transistors so the scaling routine must process each edge in turn.

Figure 9 shows CMOS transistor edge adjustment.

Some manufacturing processes may require transistor sizes to change by a differing amounts, depending on their original size or function in the circuit so an equivalence table may be used to adjust the scaling process to meet these restrictions.

Once the entire layout has been scaled, each layer that makes up the design must be grown or shrunk to meet the design rules of the new manufacturing process. This is achieved with a technique called hierarchical layer scaling which can grow or shrink the shapes in the circuit.

All of the shapes on a layer are merged together with a Boolean function before scaling to remove excess overlaps between shapes and maintain connections between shapes on the same layer. In order to maintain the electrical integrity of the circuit, the connections between shapes on the various layers must be maintained, even if these shapes occur at a different level in the hierarchy. If they become separated the circuit will not function, so it is essential that the layer scaler takes this into account.

The problems of layer connectivity only occur when the layer in question is to be shrunk and the data contains hierarchy. By moving all of the edges of a shape inward, they will detach from the shapes in sub-cells and this will break the electrical connectivity in the circuit.

Figure 10 is illustrative of layer shrinking breaking connectivity.

In order to remedy this the shapes in the sub-cells are copied to the top level and merged with the data at that level before the shrink is applied. Once the shrinking process is complete, the shapes from the sub-cells are applied as a "cookie-cutter" to remove any excess material.

It is also possible to hold layer data to the edge of a cell which is defined by the bounding box of the cell's data or by a shape representing the boundary. Layout data may held on the boundary of the cell in the same manner as scaling connectivity.

Figure 11 illustrates hierarchical layer shrink with connectivity.

In the example both shapes shrink but retain the connection between them. Only the non-connected edges are shrunk. Further rules may be applied to the layer scaler to restrict its operation to shapes that match given size rules, i.e. they are less than or greater than a given dimension. This allows data on the same layer to be scaled by differing amounts.

Figure 12 shows layer sizing by geometry width. In this example, segments of the shape can be shrunk if they meet size criteria. The shrunk segments stay attached to the large segment.

In order to meet all of the design rules for the migrated chip, it is necessary to make adjustments to parts of the shapes that make up the chip rather than the shapes as a whole. This can be described as "polygon edge adjustment" which examines each vertex of a shape and adjusts it according to its position relative to other shapes in the layout.

The edges to be adjusted may be defined by the shapes on an individual layer or identified for modification by Boolean functions to define their function in the circuit. Once this has been determined, the edges can be adjusted by an absolute value from their current position or relative to another edge on the same or a different layer. They may also be adjusted by a percentage of their distance to another edge on the same or a different layer.

Figure 13 shows edge adjustment for transistors.

All integrated circuit layouts use contact and via holes in dielectric layers to allow routing layers to connect the circuit's components. These are typically square shapes with a size and spacing defined in the technology's design rules.

Contact and via shapes may be scaled as above. Alternatively, the existing contacts and vias are removed and replaced with arrays of new shapes conforming to the new design rules. These may either be cells that make up the contact as a single array of shapes or a series of rectangles that cover the area to be connected. This area is defined through a sequence of Boolean functions that isolate the area to be connected. The new shapes conform to the new design rules by construction rather than scaling. Contacts between other materials such as metal and polysilicon may be updated using the same techniques.

Figure 14a shows contact shapes in a layout;

Figure 14b shows removing and replacing contact shapes; and

Figure 14c shows identifying areas requiring contacts with Boolean functions.

Certain layers in an integrated circuit's layout are required to overlap other layers by an amount defined in the design rules. These layers are forced to comply with the design rules through Boolean functions or through edge adjustment as defined above.

Common examples of layer overlap include polysilicon overlap of gate and metal overlap of contact.

Figure 15 shows layer overlap.

Variations between integrated circuit manufacturing processes may mean that some layers in the original chip need to be removed and others added. Examples of this would be implant layers or isolation wells.

All shapes on superfluous layers are removed hierarchically.

New layers are defined in relation to an existing layer, possibly in conjunction with another layer, e.g. place a well around a diffusion layer but only if it is crossed by polysilicon and makes a transistor.

Figure 16 shows new well defined around existing diffusion.

Data can also be promoted to new layers such as extra routing layers. Routing information may be promoted from an existing layer up to a new layer. This will allow the layout to be compressed to take advantage of the higher routing layer overlapping transistor data.

Figure 17 shows routing information from metal 1 promoted to metal 3.

In addition to scaling data, the process migration system can remove entire cells from the old layout and replace them with new cells. These new cells may come from an existing library

such as a library of standard cells, a layout generator such as a memory compiler, or they may come from a layout that has already been migrated to a new process.

The new cells are plugged in to the space in the layout vacated by the old cells and the shapes that form the connections to the cells are moved to connect to the new circuit. The migration system can replace one cell at a time, all occurrences of a cell type or all cells.

Figure 18a shows cell swapping in a standard cell layout; and
Figure 18b shows cell swapping in a block based layout.

In replacing the cells, the system accounts for discrepancies in cell and signal names between the old cells and the new. This is done with a series of equivalence tables that track the differences in names and swap the new name for the old whenever appropriate. Using this technique, the system can swap cells from different libraries and map the interconnect accordingly.

Many chips, particularly those containing standard cells, pass geometries for circuit connection between gaps in the circuit's components. These are often referred to as "feedthrough ports" and cells may contain many of these. The swapping system accounts for these connections, even though they have no direct bearing on the components they cross, and these connections are re-routed to ensure that they do not cause short circuits when crossing the new circuit components.

Figure 19 shows standard cells containing feedthrough ports.

Once the cells have been swapped, extra routing may be added to fill in any gaps between components to ensure the electrical integrity of the circuit. It is also possible to apply a compaction program to the circuit to push the components together and remove any gaps between them. There are a variety of compaction programs available for this and the techniques they employ are beyond the scope of this patent.

Once the entire circuit or a portion thereof is migrated, it is verified using industry standard design tools. These will include a design rule checking (DRC) system and layout-versus-

schematic system (LVS). These will ensure that the newly migrated chip conforms to the new design rules and has retained the integrity of the connections within the circuit.

In addition, an interconnect timing analyser may be applied at any time to check the layout will perform correctly in the new manufacturing process. This may be applied after general scaling as a rough guide to the circuits performance in the new process. even though it does not conform to the new design rules. A more accurate simulation will be available once the migration process is complete.

When the layout migration is completed and the new chip has passed verification, it may be delivered in an industry standard format such as GDSII or CIF.

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Figure 1.
Circuit hierarchy
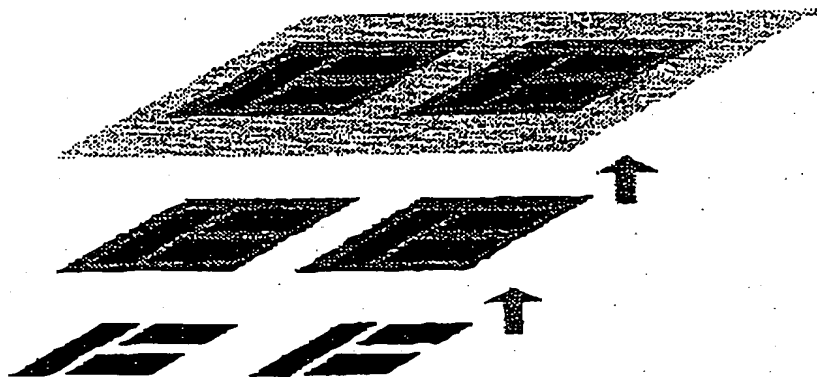
Building blocks of a circuit are placed in to larger
blocks which can be placed again in to yet larger blocks.

Figure 2.
Variable Rule Examples
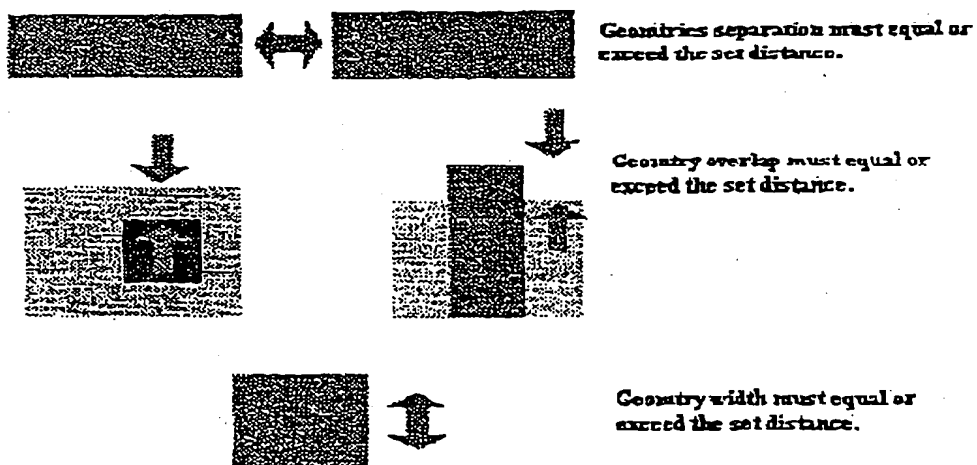
Geometries separation must equal or
exceed the set distance.

Geometry overlap must equal or
exceed the set distance.

Geometry width must equal or
exceed the set distance.

Figure 3.
Fixed geometry values.

Certain geometry dimensions must
equal a fixed value.

Transistor width and length are
defined to a fixed value.
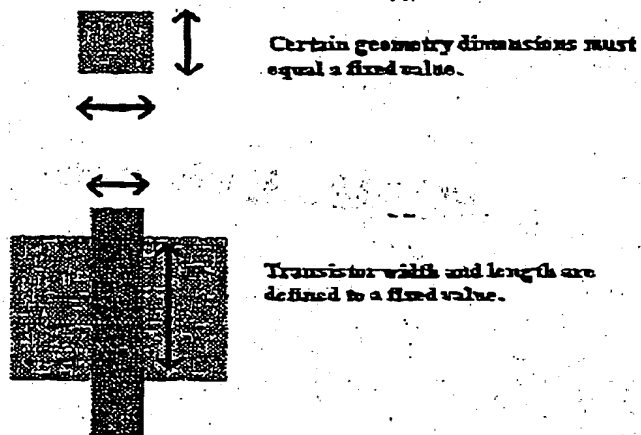
Figure 4.
Interconnect spacing.

↕ Geometry width.
↓ Geometry spacing.
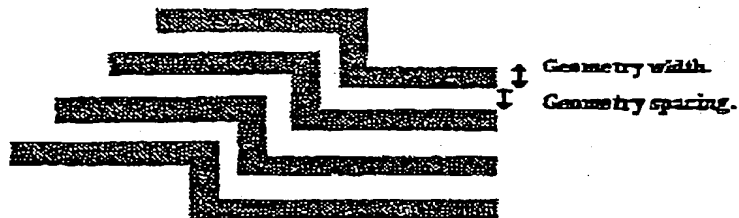
Figure 5.
Via geometries and arrays.

Via geometries between two layers   Layer 1   Via   Layer 2

3 X 2 array of via geometry.
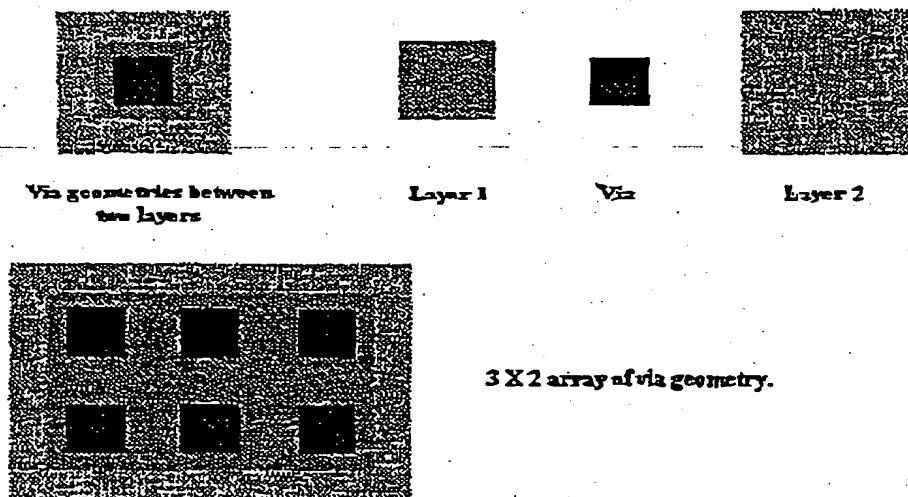
Fig 6a.
CMOS Transistor Geometry.
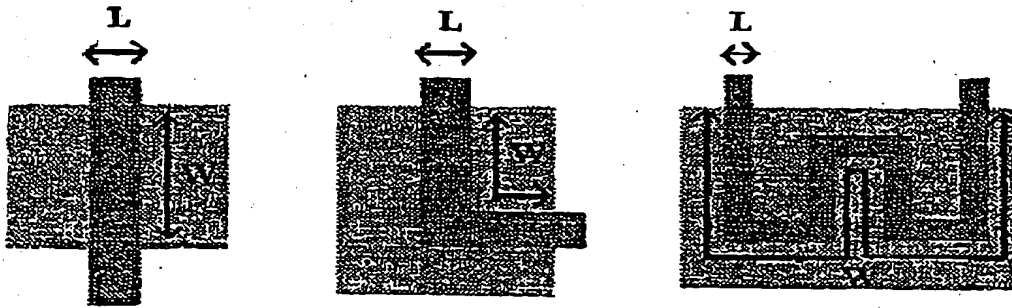
W = Transistor width

L = Transistor length

Fig 6b.
Critical dimensions when scaling CMOS Transistor Geometries.

A   B   C   D   E
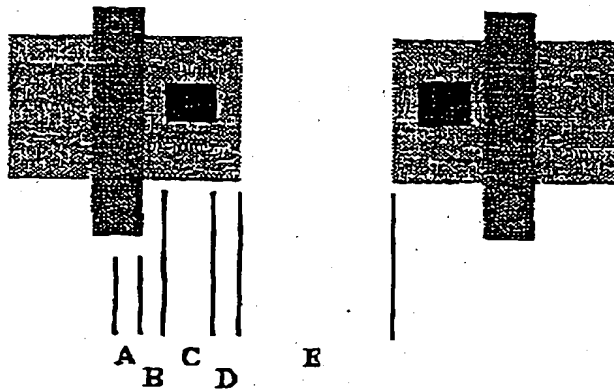
Fig 7a.
General scaling of cells.
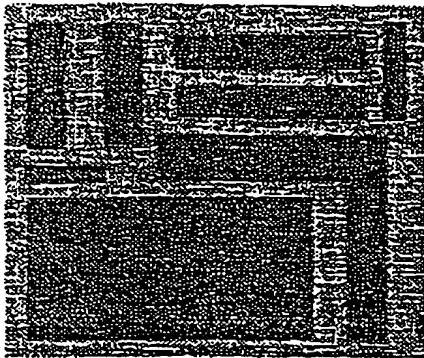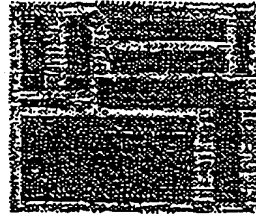
Original chip.   Scaled chip.

New dimensions = Old dimensions * Scaling factor

Figure 7b.
Scaled shapes
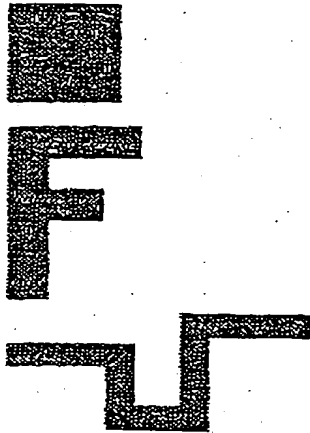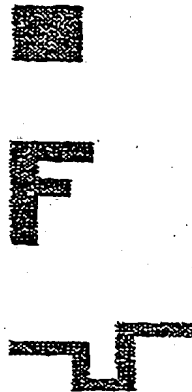
Original shapes.   Scaled shapes.

New dimensions = Old dimensions * Scaling factor

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Figure 8.
CMOS Transistor Definition.
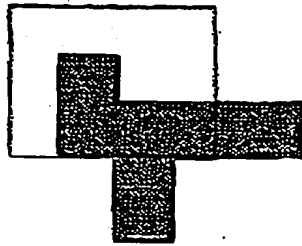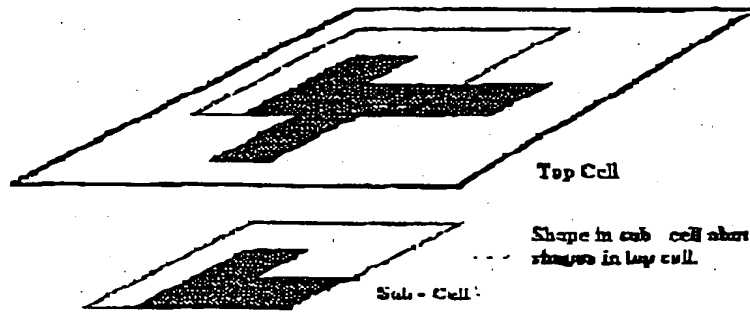
Gate Length

Gate Width

Diffusion

Polysilicon or
Metal

A CMOS transistor is
defined as polysilicon
or metal over diffusion
separating two connections
(A and B).
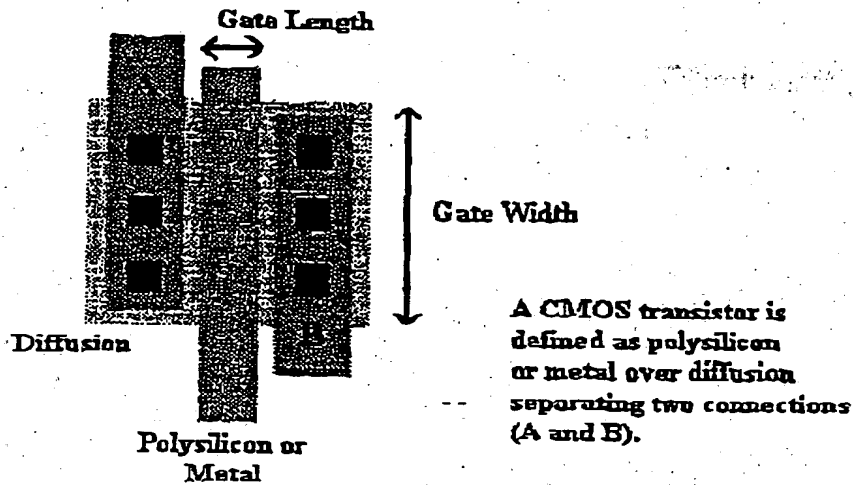
Figure 9.
CMOS Transistor Edge Adjustment.

Moving these edges adjusts
the transistor's length.

Moving these edges adjusts
the transistor's width.
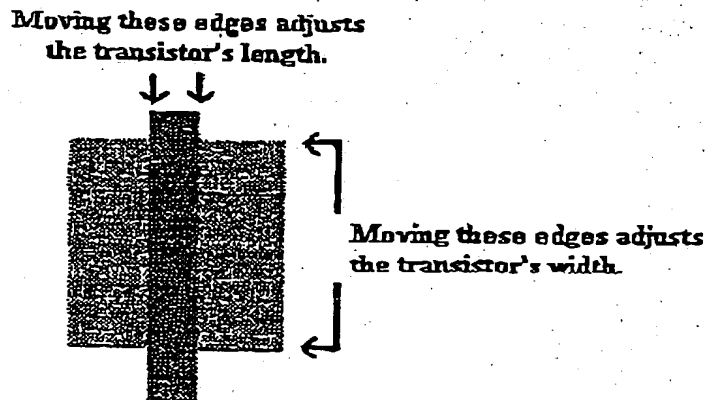
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Figure 10.
Layer Shrinking Breaking Connectivity

Top Cell

Shape in sub cell above
shapes in top cell

Sub - Cell
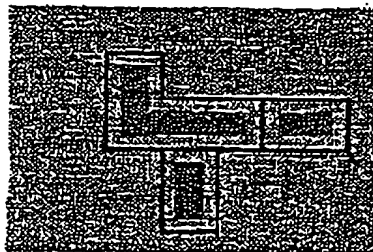
If all shapes shrink they
will become detached
from each-other.

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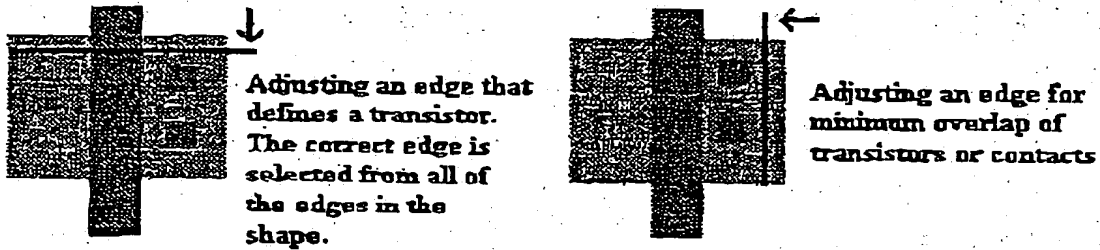## Figure 11.
Hierarchical Layer Shrink With Connectivity.

Boundary of sub-cell

Extent of original shapes.

All shapes shrink but retain the connectivity between them.

Only the non-connected edges are shrunk.
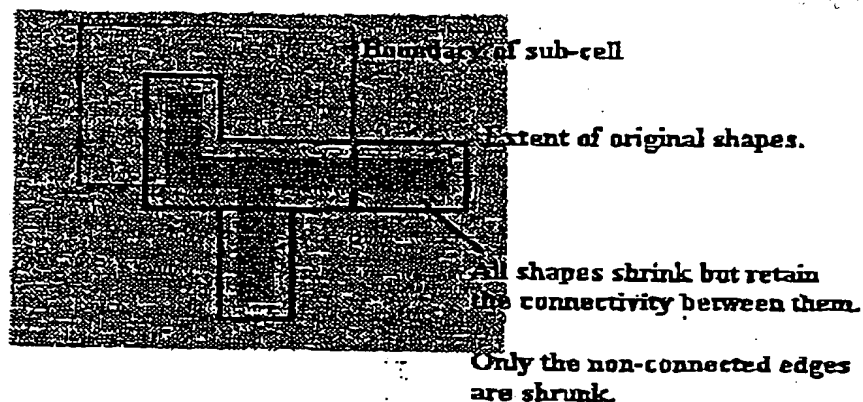
Figure 12.
Layer sizing by geometry width.

Original shape

X1

Segments of the shape can be shrunk to meet the size criteria.

| X2 | | X2 |

Modified shape

X1

Dimension X2 has shrunk to X3. Dimension X1 is unaffected.

X3   X3

The shrunk segments stay attached to the larger segment.
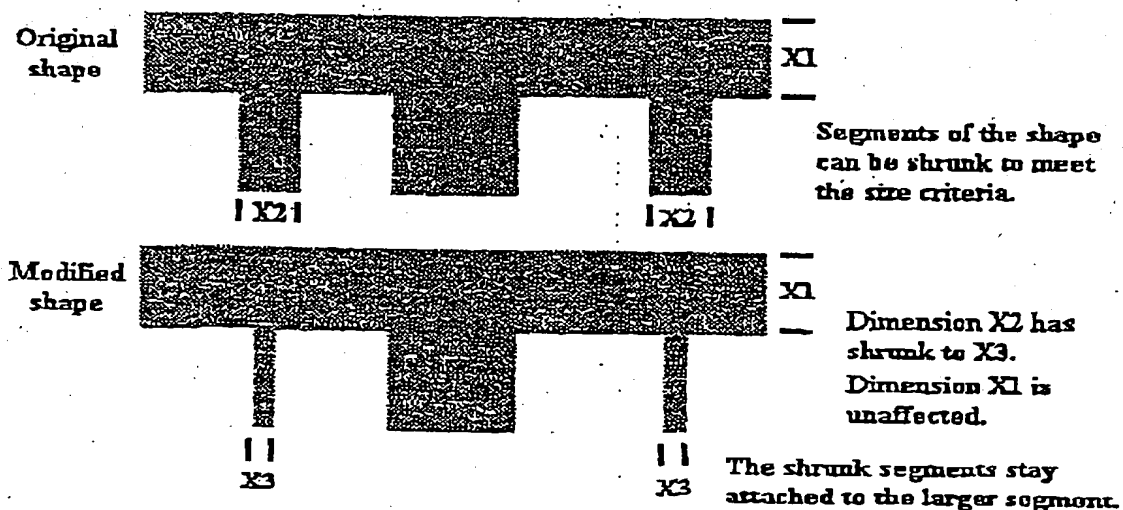
Figure 13.
Edge Adjustment for Transistors

Adjusting an edge that defines a transistor. The correct edge is selected from all of the edges in the shape.

Adjusting an edge for minimum overlap of transistors or contacts

Figure 14.
Contact removal and replacement.

Old contact shapes.   New contact shapes.   Defined area for contacts.

Old contacts are identified.

Old contacts are removed and replaced with new ones.

Contacts are placed in an area defined by boolean functions.

A   B   C
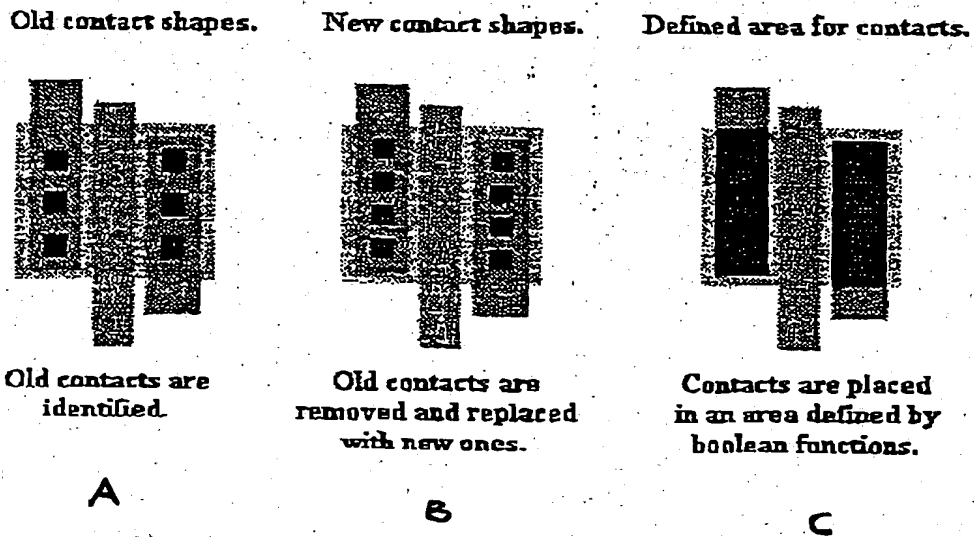
Figure 15.
Defining Layer Overlap.

Polysilicon must overlap
diffusion by a minimum of
a fixed distance.

Diffusion

Polysilicon
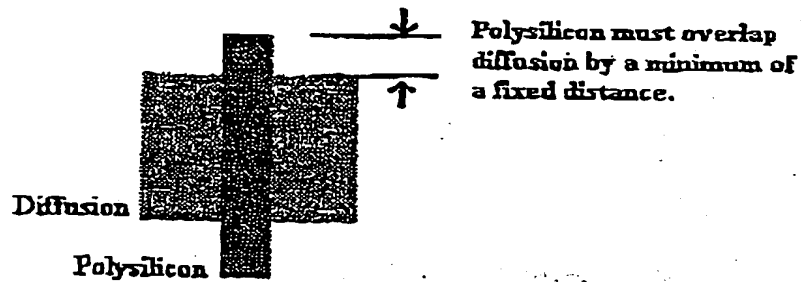
Figure 16.
Adding layers defined by existing layers.

Diffusion in
transistor

Diffusion outside
transistor

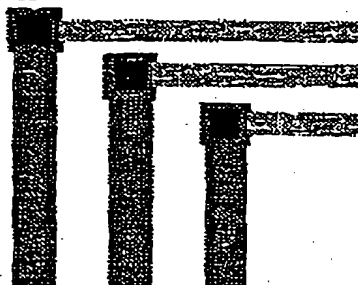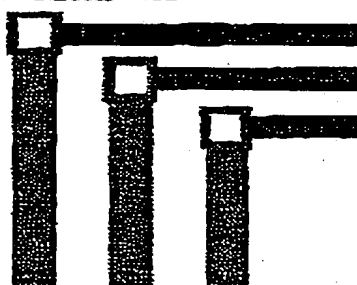New layer is only added
around the diffusion that
is part of the transistor.
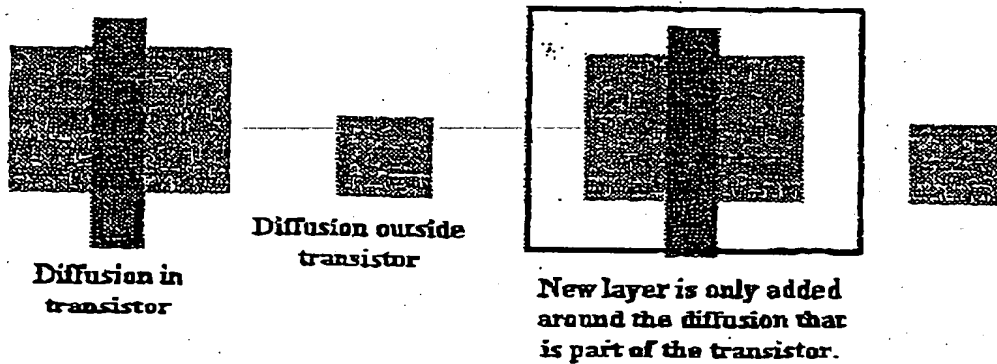
Figure 17.
Moving routing data between layers.
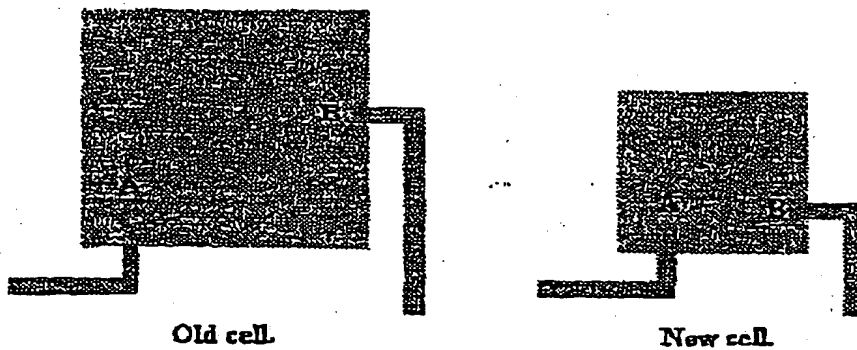
Metal1 - Metal2 via   Metal2 - Metal3 via

Metal 1
routing

Metal 3
routing

Routing information on metal 1 is promoted to metal 3
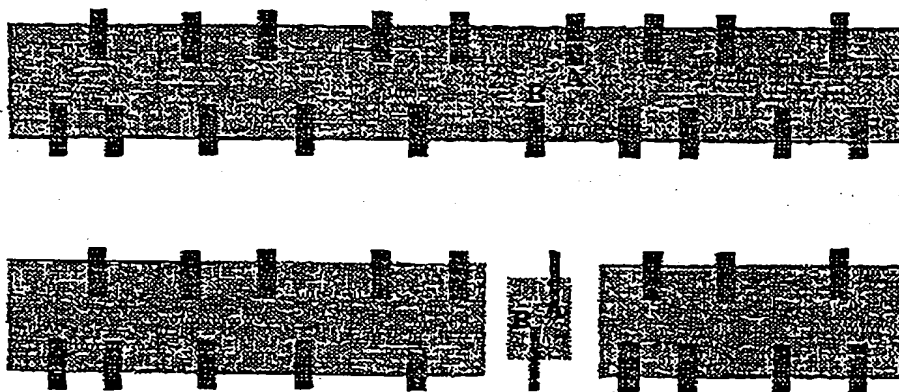and the vias are changed accordingly.

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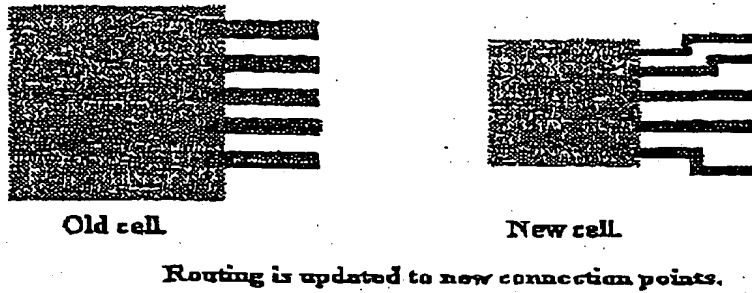
Figure 18a
Cell Swapping in a Standard Cell Layout.

Old cell.   New cell.

The new cell replaces the old and the routing to the connections
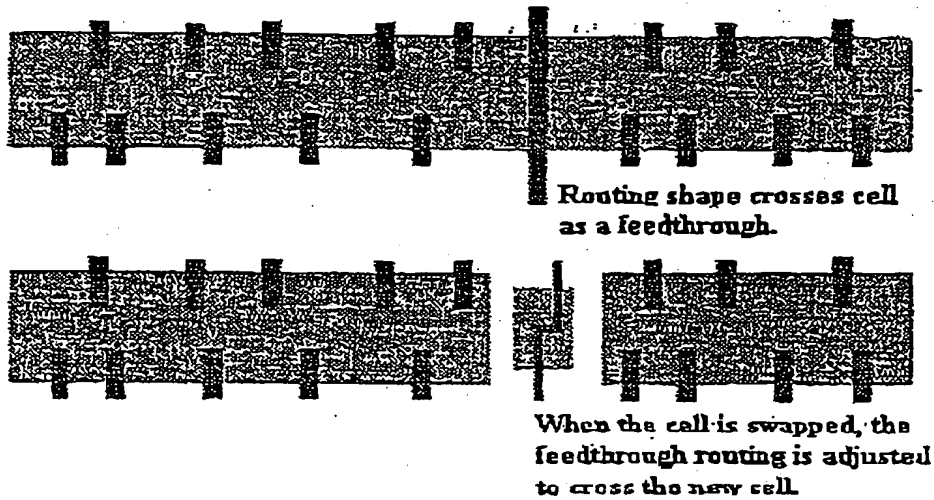A & B is updated to new positions.

Data can be updated for individual cells, by cell type
or for all cells. The routing is updated for each cell modified.

Figure 18b
Cell Swapping in a Block Based Layout.

Old cell

New cell

Routing is updated to new connection points.

Figure 19.
Standard Cells With Feedthrough Ports.

Routing shape crosses cell
as a feedthrough.

When the cell is swapped, the
feedthrough routing is adjusted
to cross the new cell.

PCT/GB00/02256

WDL

21-6-00